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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,733	07/24/2003	Tetsuya Nitta	67161-073	8046

7590 01/13/2005

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,733	NITTA ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-18* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed 10/25/04 has been entered. Claim 14 has been cancelled; no new claims are introduced.

Response to Arguments

2. Applicant's arguments filed 10/25/04 have been fully considered but they are not persuasive.

3. Applicants argue that the prior art fails to teach or fairly suggest all the elements either explicitly or inherently. Specifically, Applicants argue that Hayashi (JP 6-318561) does not teach the mask having the smaller opening ratio is used for fabricating the semiconductor element of a higher breakdown voltage. Furthermore, Applicants argue that Minato et al. ("Minato") US PG-Pub 2003/0132450 does not disclose impurity concentration of the drain of the MOS transistor.

4. In response to Applicant argument that Hayashi does not disclose all the elements recited in the claim, Hayashi discloses a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements including an implantation mask 2/3 being used that includes a portion corresponding to the drain of said one semiconductor element and having a first opening ratio A as well as a portion corresponding to the drain of said another semiconductor element and having a second opening ratio A' different from said first opening ratio. It is held, absent evidence to the contrary that the mask having the smaller opening ratio is used for fabricating the semiconductor element of a higher breakdown voltage. See In re Best, 195 USPQ 428 (CCPA 1977) and In re Fitzgerald, 205 USPQ (CCPA 1980).

5. In response to applicant's argument that Minato fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., impurity concentration of the drain of the MOS transistor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 13 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (JP 6-318561). 13.

Hayashi discloses in figs. 1-4 a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer and each having a source of a first-conductivity-type semiconductor, a drain 44 of the first-conductivity-type semiconductor and a body region 37/38 of a second-conductivity-type semiconductor between said source and said drain, comprising the steps of: implanting impurities concurrently into at least a predetermined part of the drain of one semiconductor element and into a predetermined part of the drain of another semiconductor element, an implantation mask 2/3

being used that includes a portion corresponding to the drain of said one semiconductor element and having a first opening ratio A as well as a portion corresponding to the drain of said another semiconductor element and having a second opening ratio A' different from said first opening ratio; wherein said one semiconductor element has a breakdown voltage higher than that of said another semiconductor element, and said implantation mask being used has said first opening ratio smaller than said second opening ratio; and annealing said integrated semiconductor device after said step of implanting impurities to diffuse said impurities.

As for claim 16, Hayashi discloses in fig. 4 masking portions and openings in the shape of stripes, and said implantation mask is used by being placed with said stripes arranged in the direction parallel to a carrier path from the source to the drain of said semiconductor elements.

As for claims 17 and 18, Hayashi discloses in fig. 4 an implantation mask being used is a mesh/dot implantation mask having dot-like openings dispersed in a masking portion.

5. Claims 13 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Minato.

Minato discloses (see page 7, par. 0113 and figs. 100-116) a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer and each having a source 6 of a first-conductivity-type semiconductor, a drain 3 of the first-conductivity-type semiconductor and a body region 5 of a second-conductivity-type semiconductor between said source and said drain, comprising the steps of: implanting impurities concurrently into at least a predetermined part of the drain of one semiconductor element and into a predetermined part of the drain of another semiconductor element, an implantation mask 41 being used that includes a portion corresponding to the drain of said one semiconductor element and having a first opening ratio as well as a

portion corresponding to the drain of said another semiconductor element and having a second opening ratio different from said first opening ratio (par. 0112 and claim 36); wherein said one semiconductor element has a breakdown voltage higher than that of said another semiconductor element, and said implantation mask being used has said first opening ratio smaller than said second opening ratio; and annealing (par. 0441) said integrated semiconductor device after said step of implanting impurities to diffuse said impurities.

As for claim 14, Minato discloses (see par. 0276 and par. 0112 and claim 36) said one semiconductor element has a breakdown voltage higher than that of said another semiconductor element, and said implantation mask being used has said first opening ratio smaller than said second opening ratio.

As for claim 15, Minato discloses (pars. 0396 and 0404) one semiconductor element being adjacent to said another semiconductor element, and said method further comprising the step of providing, in said semiconductor layer, a wall-shaped element-isolation film 23 for isolating said one semiconductor element from said another semiconductor element, prior to said step of implanting impurities.

As for claim 16, Minato discloses (pars. 0396 and 0404) masking portions and openings in the shape of stripes, and said implantation mask is used by being placed with said stripes arranged in the direction parallel to a carrier path from the source to the drain of said semiconductor elements.

As for claims 17 and 18, both further limitations defined by these claims fail to further limit the method making but only limit its device structure.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
January 9, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800